UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,678	08/18/2003	Sundeep M. Bajikar	42P16632	4611

8791 7590 03/26/2007

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
WILLIAMS, KENT L	
ART UNIT	**PAPER NUMBER**
2139	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/643,678	BAJIKAR ET AL.	
	Examiner	Art Unit	
	Kent L. Williams	2139	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *17 January 2006; 20 June 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed, which is accomplished. However, the Examiner feels that other features (not claimed) should be presented within the title of the invention.

The following title is suggested: "Low pin count, universal serial, and peripheral component interconnect docking bus architectures for a trusted platform."

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 2 and 5-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Krancher et al. (U.S. Patent No. 6,799,237 B2).

Claim 1. A computer system, comprising: - a chipset; a bus coupled to the chipset to communicate a trusted data cycle to an internal component of the computer system

[Column 4, lines 1-40]; and a circuit coupled to the bus that prevents a device external to the computer system from accessing the trusted data cycle [Column 5, lines 53-65].

Claim 2. The computer system of claim 1, wherein the bus is a Low Pin Count bus [Column 4, line 40].

Claim 5. The computer system of claim 1, wherein the component maintains a protected path between the chipset and a keyboard [Column 4, lines 46-50 and background section of the instant application (regarding 'protected space'); The protected path between keyboard and/or the mouse is created when the system bus is decoupled from the external bus].

Claim 6. The computer system of claim 1, wherein the computer system is a notebook computer [Column 4, lines 1-6].

Claim 7. A circuit, comprising: means for transmitting data on a Low Pin Count (LPC) bus [Column ##, lines ##; Test]; and means for preventing trusted data cycles on the Low Pin Count (LPC) bus from being accessed by an unauthorized component [Column ##, lines ##; Test].

Claim 8. The circuit of claim 7, further comprising: means for connecting an external device to a notebook computer [Column 4, lines 63-67].

Claim 9. The circuit of claim 7, further comprising: means for monitoring data cycles on the LPC bus [Column 5, lines 35-53 and Column 5 lines 53-67; Also, monitoring the data cycles is the control of the 'quick switches,' which are operable from signals presented on the bus ('output signals from the GPIO')].

Claim 10. A method, comprising: monitoring a chipset of a computer system for communication of trusted data cycles on a bus [Column 4, lines 1-40]; and preventing the trusted data cycles from being available to a component external to the computer system [Column 5, lines 53-65].

Claim 11. The method of claim 10, wherein trusted data cycles begin with a "0101" value [Column 5, line 63; Any bit patter, by definition, is a plurality of output signals – despite Krancher et al. not disclosing the use of a specific bit pattern, they have taught the use of *all* bit patterns].

Claim 12. The method of claim 10, further comprising: communicating trusted data cycles between the chipset and a first component [Figure 2, block 106 and 108 with 122].

Claim 13. The method of claim 12, wherein the communication between the chipset and the first component is in plaintext format [Any bus system within a notebook computer will communicate data cycles (inclusive trusted cycles) in plaintext format. See Background and Figures 1 and 2].

Claim 14. The method of claim 10, further comprising: communicating trusted data cycles between the chipset and a second component [Figure 2, block 106 and 110 with 122].

Claim 15. The method of claim 14, wherein the communication between the chipset and the second component is in plaintext format [Rejected for the same reasons as Claim 13].

Claim 16. The method of claim 15, wherein the second component maintains a protected path between the chipset and a keyboard, wherein keystroke data is communicated by the chipset to protected memory and trusted applications [Column 4, lines 46-50].

Claim 17. The method of claim 15, wherein the second component maintains a protected path between the chipset and a mouse, wherein pointer data from the mouse is communicated by the chipset to protected memory and trusted applications [Column 4, lines 46-50].

The following is supplementary to the rejection above:

Claims 1, 2, 6, 7-9, 10-15 recite the limitations of a system containing a "chipset" (as understood in the art to mean Input/Output Controller Hub), a bus (collection of data signal lines) to transmit a "trusted data cycle" to a component or components, and a circuit to prevent an "external device" from accessing a "trusted data cycle" by monitoring the bus for a "trusted data cycle" signal, where the bus is a Low Pin Count (LPC) bus and the system is a notebook computer. Claims 7-9 further recite the limitations "means for," invoking 35 U.S.C. 112, sixth paragraph to "read in" slightly variable structures from the specification pertaining to a notebook computer and its respective bus communications systems as is known in the art, and "connecting an external device to a notebook computer" (e.g., a "laptop docking station"). Claim 11 further recites that said "trusted data cycle" is indicated by a specific bit pattern. Claims 12-15 further recite that a "trusted data cycle" is communicated to a first and second components coupled to said bus in plaintext format. Krancher et al. teach that their

invention is directed toward the general system of a notebook computer having a bus system with varying interfaces and circuits, inclusive laptop docking architectures (Column 4, lines 1-30). Krancher et al. teach that their invention is for use with any bus system, stated as, "The preferred embodiment of notebook **200** further includes a second bridge logic device, known in the art as Input/Output Controller Hub (ICH) **64**. The ICH **64** couples or bridges the primary expansion bus **60** to other secondary expansion buses...[that] may include...a low pin count (LPC) bus [among all others]. (Column 4, lines 32-40)." Most importantly, Krancher et al. teach the use of signals (inherently in the form of data cycles as it pertains to a bus) to indicate that communication between the laptop bus and the external bus (or "external device") should be denied, taught as, "More particularly, and still referring to FIG. 1, the preferred embodiment comprises a plurality of quick switch devices **86** that allow each of the bus signals of the PCI bus **70**, and each of the serial signals of the I^2C serial bus **84**, to be selectively coupled to the physical pins (not shown) of the connector **82**. (Column 5, lines 53-58)." Decoupling of physical pins, by the ability of "selectively coupling," denies the external bus (and subsequently the external device) from "accessing" the data (or "data cycle") on the bus during said decoupling. Krancher et al. teach the use of a particular signal within a "data cycle" to indicate decoupling of the bus data from the external bus/device as, "That plurality of quick switches **86** is preferably controlled by a plurality of output signals from the general purpose input/output (GPIO) **88**, available on the Super I/O. Use of the GPIO **88** on the Super I/O **74**, however, is merely exemplary. One of ordinary skill in the art could fashion many ways to control the quick switches **86**

through the use of other output signals available within the notebook computer **200**. (Column 5, lines 60-68 through column 6, lines 1-2)." By definition, the bit pattern '0101' ***is*** a "...plurality of output signals from the general purpose input output... (Column 5, lines 63)." Any bus system within a notebook or desktop computer system will "communicate data cycles" (inclusive "trusted data cycles" if they are indicative of decoupling the external bus/device) between pluralities of components using plaintext (or unencrypted data). Please see the Background section and Figures one & two of Krancher et al.

Claims 5, 16 and 17 recite the limitations of "maintaining a protected path between the chipset and keyboard & mouse." The chipset is also known as the Input/Output Controller Hub, mentioned supra. Krancher et al. teach a "protected path" between the chipset (Input/Output Controller) and the keyboard & mouse via the use of decoupling the bus from external bus'/devices during a signal cycle of the bus indicating to do so ("trusted data cycle"), as discussed, and "Also attached to the LPC bus **72** is a Super Input/Output (Super I/O) controller **74**, which controls many system functions, including interfacing with various input and output devices such as keyboard **76** and mouse **78**. (Column 4, lines 46-50)." Also, any memory located on said protected "path"/bus would, indeed, be "protected" memory. The Examiner wishes to note that the background section of the instant application contains pertinent admitted prior-art regarding "protected space," which is inclusive of protected memory and/or "paths" (A.K.A. bus') together to form a "protected space"/"protected system."

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 3, 4 and 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krancher et al. (U.S. Patent No. 6,799,237 B2) and "Trusted Computing Platform Alliance (TCPA) Main Specification Version 1.1b," 22 February 2002, referred to as "TCPA" hereinafter.

Claims 3, 4 and 18-22 recite the limitations that one component connected to the bus system has "protected memory storage" and "platform authentication." Claims 18-22 further recite that the component protects data by encryption/decryption using hardware, can give platform attestation via a "system ID request" involving a third party verification (A.K.A. Certificate Authority), and can give root of trust measurements via "merging data with the computer system's configuration values. It should be noted that

claims 3,4 and 18-22 recite an entirely different invention that could be considered patentably distinct.

> **Claim 3.** The computer system of claim 1, wherein the component provides protected memory storage [TCPA, Page 5, §2.3.1].
> **Claim 4.** The computer system of claim 1, wherein the component provides platform authentication [TCPA, Page 6, §2.3.1-§2.3.2].
> **Claim 18.** The method of claim 12, wherein the first component protects secret data of the computer system by encrypting the secret data [TCPA, Page 7, §2.5].
> **Claim 19.** The method of claim 18, wherein the secret data is decrypted by hardware of the computer system [TCPA, Page 7, §2.5].
> **Claim 20.** The method of claim 18, wherein the first component merges data with the computer system's configuration values [TCPA, Pages 2-3, §2.2].
> **Claim 21.** The method of claim 18, wherein the first component requests for a system identification request [TCPA, Page 10, §2.6.2].
> **Claim 22.** The method of claim 21, wherein a trusted third party chip verifies the computer system's identification and sends a response to the first component [TCPA, Page 10, §2.6.2].

Krancher et al. teach the systems and methods previously presented. However, Krancher et al. fails to teach a Trusted Platform Module (TPM) present on the bus system of the notebook computer. TCPA teaches a TPM on a computer bus capable of platform attestation (TCPA, page 6, §2.3.1-§2.3.2), root of trust (TCPA, pages 2-3, §2.2), and protected storage (TCPA, page 5, §2.3.1) with hardware encryption (TCPA, page 7, §2.5).

It would have been obvious at the time the invention was made to one having ordinary skill in the art to use the features of a Trusted Platform Module (given by the TCPA specification) in tandem with the notebook computer bus securing means of Krancher et al. because doing so would further improve the security of said notebook computer. Further, the TCPA specification states, "This specification defines a trusted Subsystem that is an integral part of each platform, and provides functions that can be

used by enhanced operating systems and applications. The Subsystem employs cryptographic methods when establishing trust, and while this does not in itself convert a platform into a secure computing environment, it is a significant step in that direction. (Page 1)." Another "step in that direction" would be to include the bus securing means of Krancher et al.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 1, 2, 6 and 7-10 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 13 and 16 of U.S. Patent No. 6,871,252. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are both drawn to preventing data on a computer

system bus from being compromised by denying propagation of said data to an external bus and/or component. The instant application claims a circuit to prevent an external device from accessing a data cycle on the computer system bus. The U.S. Patent claims pull-up and pull-down resistors with a switch to prevent an external device from accessing a data cycle on the computer system bus.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent No. 5,748,888 defines a method and apparatus for providing a secure and private keyboard communications in a computer system. Please note U.S. Patent No. 6,868,468, as provided by the applicant. Of particular interest to the applicant, please note Application No. 11/061,146 (U.S. Application Publication No. 2006/0190653.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kent L. Williams whose telephone number is 571-270-1376. The examiner can normally be reached on Mon-Fri 7:00-4:30 with Alternate Fridays Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz R. Sheikh can be reached on 571-272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kent Williams
3/7/2007

Taghi T. Arani
Primary Examiner
3/16/07